Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Collector Q1**
2. **Base Q1**
3. **Emitters Q1 and Q2**
4. **Base Q2**
5. **Collector Q2**
6. **Base Q3**
7. **Emitter Q3**
8. **Collector Q3**
9. **Base Q4**
10. **Emitter Q4**
11. **Collector Q4**
12. **Base Q5**
13. **Emitter Q5 (and SUBSTRATE)**
14. **Collector Q5**

**.040”**

**.040”**

**9 8 7**

**6**

**5**

**4**

**3**

**2**

**10**

**11**

**12**

**13**

**14 1**

**MASK**

**REF**

**SS45**

**NOTE:**

**The SUBSTRATE must be connected to the most negative point in the external circuit to maintain isolation between trasistors and to provide for normal transistor action.**

**Top Material: TiW-AlSi**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: See note**

**Mask Ref: SS45**

**APPROVED BY: DK DIE SIZE .040” X .040” DATE: 4/6/23**

**MFG: SILICON SUPPLIES THICKNESS .018” P/N: SIS3046**

**DG 10.1.2**

#### Rev B, 7/19/02